Aasheesh Kolli

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Nationality: Indian (permanent resident of USA)

Research interests

My current research focuses on maximizing the benefits of persistent memories through novel memory system architectures, programming interfaces, and software optimizations. Broadly, I am interested in designing useful programming interfaces and efficient hardware implementations to facilitate the adoption of emerging technologies.

Education

- **Ph.D. Candidate, Computer Science and Engineering** (Sep 2011 – Present)
  University of Michigan - Ann Arbor, *Dissertation title:* Getting ready for the advent of persistent memories
  Advisor: Prof. Thomas F. Wenisch, *Expected Graduation Date:* May 2017
- **M.S. Computer Science and Engineering** (Sep 2011 – Dec 2012)
  University of Michigan - Ann Arbor (**GPA:** 4.0/4.0)
- **B.E.(Hons), Electrical & Electronics + M.Sc.(Hons), Economics** (Aug 2006 – May 2011)
  Birla Institute of Technology & Science - Pilani, India (**GPA:** 9.08/10.0)
  Thesis Advisor: Prof. Rajeev Balasubramonian, University of Utah (Jul 2010 - May 2011)

Academic experience

Graduate Student Research Assistant *University of Michigan, Ann Arbor* (Sep 2011 – Present)

- **Memory persistency:** Future computing systems are expected to place persistent memories (PMs) alongside DRAM on the memory bus, allowing durable storage access to programmers via processor loads and stores, a paradigm shift in how durable storage is accessed. This work focuses on developing novel memory system architectures, programming interfaces, and software optimizations to fully exploit the benefits of PMs.
- **Hardware acceleration:** Rapidly processing text data is critical for many technical and business applications. This work develops a custom hardware accelerator that processes text at memory bandwidth speeds, outperforming traditional software solutions (e.g. grep) by up to 20x.
- **Instruction prefetching:** L1 instruction misses remain a critical performance bottleneck for server applications. This work simplifies and reduces the energy requirements of accurate instruction prefetching by exploiting the relationship between instruction misses, program contexts and the return address stack.

Undergraduate Intern *University of Utah, Salt Lake City* (Jul 2010 – May 2011)

- **Cache management policies:** This work identifies that an application's working set can be separated into different regions based on frequency of use and explores the idea of "intra-application cache partition" where the cache is appropriately partitioned among regions in its working set, using the CMP$im simulator.

Professional experience

Software Engineering Intern *Google, Madison* (May 2016 – August 2016)

- **Evaluation infrastructure for network protocols:** I developed an infrastructure to evaluate the throughputs and latencies exhibited by various network protocols. This infrastructure can be used to evaluate both point-to-point and distributed system configurations. This work is currently being used internally at Google.

Research Intern *HP Labs, Palo Alto* (May 2015 – May 2016)

- **Asynchronous, parallel log truncation for persistent memories:** Programming interfaces that provide failure-atomicity for persistent memory updates typically rely on some form of logging to ensure failure-atomicity. This work observes that log truncation is a performance bottleneck and parallelizes it to achieve better performance.

Research Intern *ARM, Cambridge, England* (May 2013 – Dec 2013)

- **Server workload characterization and simulator development:** This work analyzes the memory system requirements for server workloads and aided the development of an event-based DRAM memory controller in gem5.

Peer-reviewed publications

- **A. Kolli**, J. Rosen, S. Diestelhorst, A. Saidi, S. Pelley, S. Liu, P.M. Chen, T. F. Wenisch. "Delegated Persist Ordering". International Symposium on Microarchitecture (**MICRO**), Oct 2016.
  Nominated for best paper award.
- V. Gogte, **A. Kolli**, M. J. Cafarella, L. D'Antoni, T.F. Wenisch. "HARE: Hardware acceleration for regular expressions". International Symposium on Microarchitecture (**MICRO**), Oct 2016.
- **A. Kolli**, S. Pelley, A. Saidi, P.M. Chen, T.F. Wenisch. "High-performance Transactions for Persistent Memories". International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), Apr 2016.
- J. Izraelevitz, Terence Kelly, **A. Kolli**. "Failure-Atomic Persistent Memory Updates via JUSTDO Logging". International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), Apr 2016.
- **A. Kolli**, S. Pelley, A. Saidi, P.M. Chen, T.F. Wenisch. "Persistency programming 101". Non-Volatile Memory Workshop (**NVMW**), Mar 2015.
- A. Hansson, N. Agarwal, **A. Kolli**, A.N. Udipi, T.F. Wenisch. "Simulating DRAM controllers for future system architecture exploration". International Symposium on Performance Analysis of Systems and Software (**ISPASS**), Mar 2014.
- **A. Kolli**, A. Saidi, T.F. Wenisch. "RDIP: Return-address-stack Directed Instruction Prefetching". International Symposium on Microarchitecture (**MICRO**), Dec 2013.

Patents

- A. Saidi, T.F. Wenisch and **A. Kolli**. "Prefetching based upon return addresses"
  US Patent Pend.
- S. Diestelhorst, **A. Kolli**, A. Saidi, P.M. Chen, T.F. Wenisch. "Controlling memory access to non-volatile memory"
  US Patent Pend.
- J. Izraelevitz, **A. Kolli**, T.P. Kelly, C.B. Morrey III, "Resuming execution in response to a failure"
  US Patent Pend.
- T.P. Kelly, C.B. Morrey III, D. Chakrabarti, **A. Kolli**, Q. Cai, A.C. Walton, J. Izraelevitz, "Register store"
  US Patent Pend.

Honors and awards

- Publication nominated for best paper award at IEEE MICRO'16
- Rackham Graduate Fellowship at University of Michigan (2011 - 2012)
- President, Institution of Engineering and Technology - Student chapter at BITS-Pilani (2009-2010)

Grants

- *Contributed to writing* "Memory Persistency: programming paradigms for byte-addressable, non-volatile memories" National Science Foundation (Award #1525372), Amount awarded: **$499,996.00**

Press

- Baking Specialization into Hardware Cools CPU Concerns, *Next Platform, 09/21/16*

Talks

- "Invited guest lecture on persistent memory systems"
  EECS 598 at Univ. of Michigan (for Prof. Reetuparna Das), October 2016
- "Delegated Persist Ordering"
  Int'l Symposium on Microarchitecture (MICRO), October 2016
- "Gearing up for the advent of persistent memory"
  Google, July 2016
- "High-performance transactions for persistent memories"
  Int'l Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Apr 2016
- "High-performance transactions for persistent memories"
  Non-Volatile Memories Workshop (NVMW), March 2016
- "Persistency programming 101"
  Non-Volatile Memories Workshop (NVMW), March 2015
- "RDIP: Return-address-stack Directed Instruction Prefetching"
  Int'l Symposium on Microarchitecture (MICRO), December 2013

Teaching

- **Instructor**, Introduction to Computer Organization, University of Michigan, Fall '16
- **Graduate Student Instructor**, Parallel Computer Architectures, University of Michigan, Winter '13
- **Undergraduate Teaching Assistant**, Circuits and Signals, Birla Institute of Technology & Science, Winter '09

Service

- Co-organizer for the CS KickStart hardware lab, a workshop aimed at improving gender diversity in CS through increased female enrollments.
- Moderator for the CELAB reading group (2015-16), a reading group that meets weekly to discuss recent papers from top-tier computer architecture conference.

References

- **Thomas F. Wenisch**
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- **Parthasarathy (Partha) Ranganathan**
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